Interface to audio ADC sampling ICs

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There are several aspects of audio converter design that are generally not well understood but have a dramatic impact on performance, both measurable and audible. Audio converter IC manufacturers generally give circuit recommendations to address these issues but rarely discuss the reasoning behind these suggestions, how performance is affected and why it is important to follow the rules.

However, once a designer has an insight into the issues, it is possible to identify the compromises that often exist in the manufacturers recommendations. This can lead to intelligent insights to lower cost, or in some instances, improve performance.

One of these areas is interfacing to the sampling networks of analog-to-digital-converters. Today's high-performance A/D converters are based on highly oversampled multi-bit delta-sigma conversion with sampling circuits that operate at frequencies several orders of magnitude beyond the audio range. An understanding of how to properly interface to these networks is probably the least understood topic in A/D systems design and remains one of the "magical" areas of audio circuit design.

ADC sampling circuits

The operation of a simplified sampling network can be broken down into two phases (**figure 1**). During the initial phase or the capture phase, switch one (SW1) is closed and switch two (SW2) is open. This allows the sampling capacitor (CIN) to charge to the voltage presented by the external analog drivers. During the second phase, SW1 is open and SW2 is closed which allows the captured charge on CIN to be transferred to the integrator as a voltage for conversion.

The repetition rate of this process is determined by the frequency of the oversampling clock and is typically 128 times the output sample rates from 16 to 50 kHz which equates to a 6.144-MHz analog sample rate for a 48-kHz output sample rate. Understanding and properly addressing the challenges presented by the high speed sampling and switching is very important to a successful design.

A representative input current waveform is shown in **figure 2**. The polarity and total charge transferred within each period is a function of the input signal amplitude, signal polarity, sampling frequency and the capacitance of the sampling capacitor. This high-speed switching, and the transient currents they create, presents an impossible load for the majority of operational amplifiers.

Consider that during the initial capture phase, the buffer amplifier is required to drive a discharged capacitor that essentially appears to be an instantaneous short circuit to Vbias. Conversely, during the conversion phase the sampling capacitor is disconnected from the buffer and the load becomes an open circuit. This process is repeated at the oversampling rate and the external buffer amplifier typically has problems with the transient load conditions when driving the sampling capacitor directly. It is rather obvious that requirements demanded by the switched capacitor loading are not typical of standard audio circuitry.

In addition to the linear sampling currents, there are several sources of nonlinear signal level dependent sampling currents within the sampling networks. Since this nonlinear current must be supplied by the signal source, this will translate to distortion if the source impedance is sufficiently large. The magnitude of this nonlinear current will vary between different converter designs and architectures and converter manufacturers generally recommend driver source resistance to be less than 100 Ω, and in many cases much less, to meet stated distortion specifications.

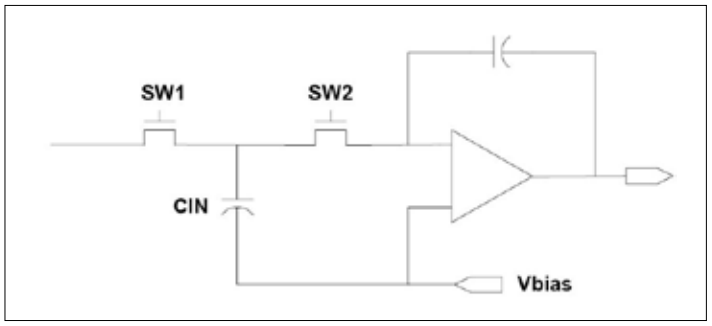

Figure 1: Simplified A/D sampling circuit.

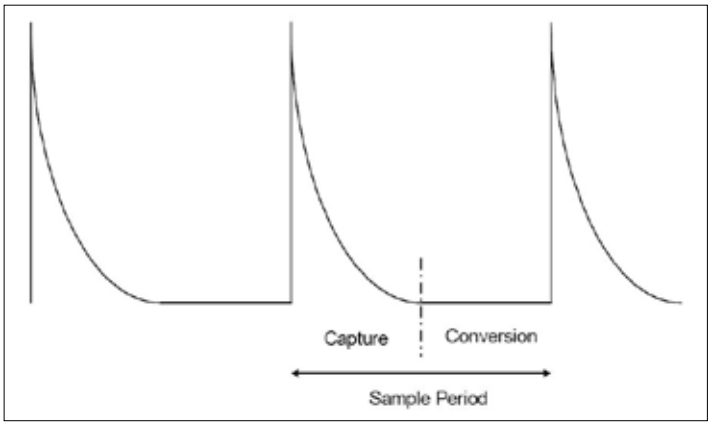

Figure 2: A/D input sampling currents.

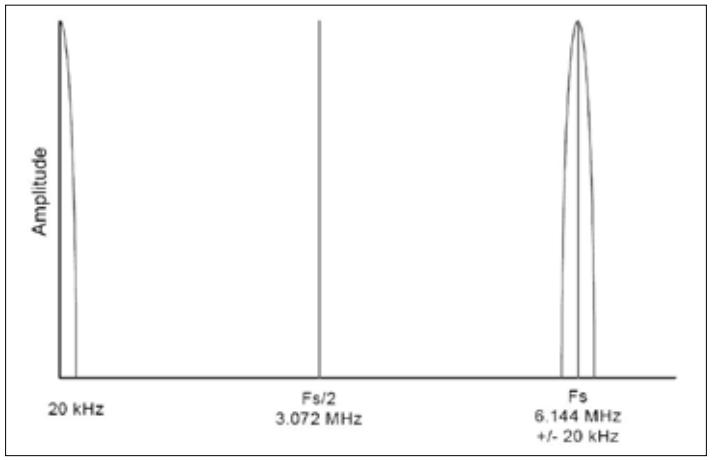

Figure 3: Oversampling A/D aliasing spectrum.

The analog sections of audio A/D converters typically operate with a single 5- or 3.3-V power supply and, as a result, the input signal must be biased at a DC voltage near mid-supply. This is shown in figure 1 where the sampling capacitor is connected to the internal bias voltage, Vbias. Differences in the quiescent voltage of the external buffer and the internal bias voltage translate to non-symmetrical currents be-

tween equal magnitude positive and negative analog signal inputs. This can have a negative impact on distortion performance and creates non-symmetrical clipping behavior.

The best remedy is to take advantage of the internally generated bias voltage that is typically available on one of the device pins. The intended purpose of this output is to provide an external capacitor to filter noise from the bias voltage. However, this pin may also be used to bias the input buffer circuits, but a word of caution. These outputs are generally not intended to supply a significant amount of current and often must be buffered prior to biasing the input circuitry. Examples of this technique are often listed in the applications sections of converter data sheets.

Anti-alias filtering requirements

It is interesting to consider the anti-alias filter requirements for highly oversampled audio A/D converters. Referring to **figure 3**, the oversampling frequency is 6.144 MHz and the Nyquist frequency is 3.072 MHz.

Recall that all frequencies above the Nyquist frequency will alias to between DC and the Nyquist frequency. However, what is generally not obvious is that the digital decimation filter will remove the frequency components above the digital filter passband and the Nyquist frequency. Therefore the frequency components that will alias into the passband exist at N times the oversampling frequency plus/minus the digital filter passband (N × 6.144 MHz ±20 kHz).

As a result of the high frequency required for aliasing to occur, it could be argued that anti-alias filtering is not required for audio since the sources of audio signals do not have sufficient bandwidth to produce signals at frequencies near the A/D oversampling frequencies. It can also be argued that filtering is required to remove extraneous high frequency noise that may have entered into the signal chain via electromagnetic interference.

In reality this argument is questionable since RF generally enters the system through the interconnecting cables and should be removed prior to the buffers. However, the least recognized and most important requirement is simply to avoid the aliasing of broadband noise that will degrade system dynamic range, which is particularly important for high dynamic range converters.

The leading A/D converters have dynamic range capabilities of 120 dB and require buffer noise contributions well below that of a 1-kΩ resistor to meet performance specs. It is a relatively challenging and expensive proposition to meet this goal over the audio frequency band.

The analog buffer circuitry preceding the A/D converter will generate noise with a frequency content that extends well beyond the oversampling frequency. Aliasing creates a mechanism for this noise, at integer multiples of the oversampling frequency, to contribute to noise within the audio band and degrade dynamic range.

Allowing the noise at 6.144 MHz ±20 kHz to alias will triple the noise within the 20-kHz passband. Fortunately it doesn't require much filtering to sufficiently limit the signal bandwidth prior to the A/D to avoid this problem and a single-pole RC filter with a corner frequency approximately a decade below the sampling frequency will attenuate broadband noise by at least 20 dB, which is sufficient (**figure 4**).

Input buffer topologies

As previously discussed, the transient loading from the sampling circuits generally causes the amplifier to operate in a nonlinear mode and exhibit ringing and/or oscillation when driving the switched-capacitor directly. A mechanism is required which isolates the amplifier from the transient switched-capacitor loading. **Figure 5** shows the opamp input buffer topology that audio A/D converter suppliers have recommended for many years to address these issues.

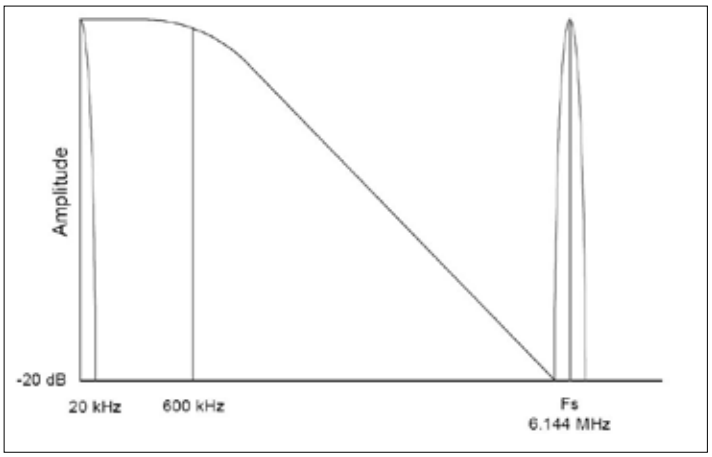

Figure 4: Oversampling A/D anti-alias filter response.

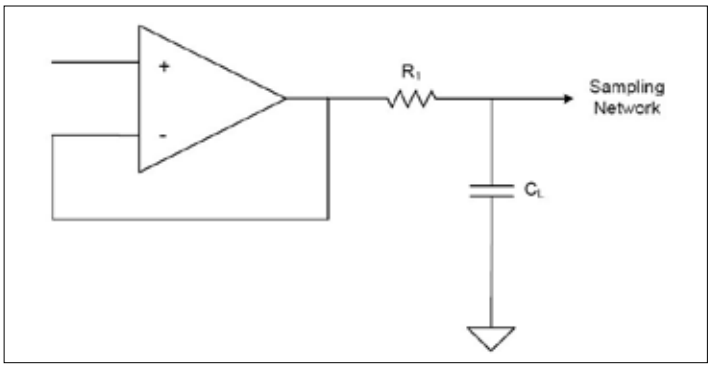

Figure 5: Classic A/D buffer topology.

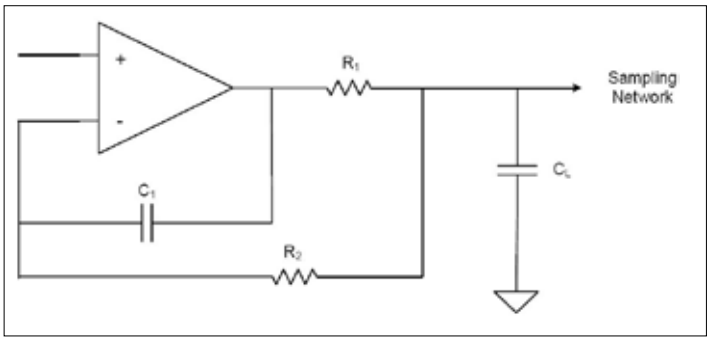

Figure 6: Compensated buffer topology.

The addition of the series resistor (R1) and the load capacitor (CL) between the opamp and the sampling network meet several of the required goals. In this configuration, the instantaneous current for the sampling capacitor is provided by CL while the average current is supplied by the operational amplifier. This greatly reduces the transient current seen by the opamp and the likelihood that the amplifier will ring or overshoot. The resistor isolates the amplifier from the transient currents and also provides the stability required to drive the large capacitive load presented by CL. In addition, the combination of R1 and CL provide the required single-pole anti-alias filter.

A/D converters manufacturers typically recommend values for R1 and CL. The recommended capacitance of CL is typically on the order of a couple of magnitudes larger than that of the sampling capacitor. This is partially to ensure that there is sufficient charge on CL to prevent a significant voltage drop when the sampling capacitor is charged. However, the exact value is often selected via a series of experiments to determine the optimum value for best performance.

The selection of an appropriate value for R1 is obviously dependent on the capacitance of CL. In addition there are other

constraints. The lower limit is determined by the requirements to isolate the amplifier from the transient switching currents and to maintain amplifier stability when driving the large capacitance of CL.

The upper limit is also set by two requirements. First the time constant of the RC circuit must be small enough to allow the load capacitor to properly charge and accurately reflect the analog input signal. Making the time constant too large can reduce settling accuracy. The second requirement relates directly to the magnitude of the nonlinear sampling currents previously discussed and the design distortion goals. Excessive resistance values for R1 directly translate to distortion.

The classic buffer topology in **figure 5** has many advantages but remains a compromise. With the relatively recent performance increases of A/D converters, these compromises have become a limiting factor. The required capacitance of CL has increased while the upper limit for R1 has decreased to meet the the dynamic range and distortion capabilities of high-performance converters. These requirements, while maintaining amplifier stability, are conflicting and the adoption of a new approach is required to match the capabilities of high-performance converters.

The attributes of the ideal buffer are a zero-ohm source impedance to the sampling network over the audio bandwidth to minimize distortion, a sufficiently high output impedance at the sample frequency to provide isolation, a single-pole anti-alias filter response and the ability to drive the large capacitance of CL while maintaining stability.

The compensated buffer topology (**figure 6**) was originally developed to stabilize an amplifier driving a large capacitive load. This circuit topology works very well for the intended purpose and it also has attributes, that are generally not discussed in the articles, that make it very nearly the ideal topology for directly driving audio A/D sampling networks. An intuitive approach is helpful to understand the circuit operation.

Within the audio passband C1 can be considered an open circuit. Notice that with C1 out of the circuit, R1 is within the feedback loop of the amplifier. In this configuration, the output impedance of the amplifier is R1 divided by the loop gain of the amplifier, which provides a very low source impedance.

At the oversampling frequency, C1 can be considered a short circuit and R1 is no longer within the feedback loop. The output impedance of the circuit becomes R1 which provides sufficient isolation at the sampling frequency. In addition, the component values may be selected to provide the required anti-alias filtering with an acceptable corner frequency.

The compensated buffer has the advantages of negligible source impedance within the audio band for minimal distortion, stability for driving large capacitive loads, isolation at the oversampling frequencies and providing the required anti-alias filtering. In addition, the circuit requires low resistance values, which minimizes noise contributions, and a very high input impedance.

Requirements for CL

Selection of the load capacitor (CL) is critical in this application. As previously discussed, CL is required as a charge reservoir for charging the sampling capacitor and as a component of the anti-alias filter. **Figure 7** shows the electrical model for a capacitor which includes the equivalent series inductance (ESL), the equivalent series resistance (ESR) and the DC leakage current (DCL). The DCL is a critical parameter for electrolytic capacitors but can be considered negligible for any type of capacitor suitable for this application.

The impedance versus frequency plot for a non-ideal capacitor is shown in **figure 8** where C is equal to 2700 pF, ESL is 1.5 nH and ESR is 0.1 Ω. Notice the effect of the inductance where the impedance reaches a minimum at the series

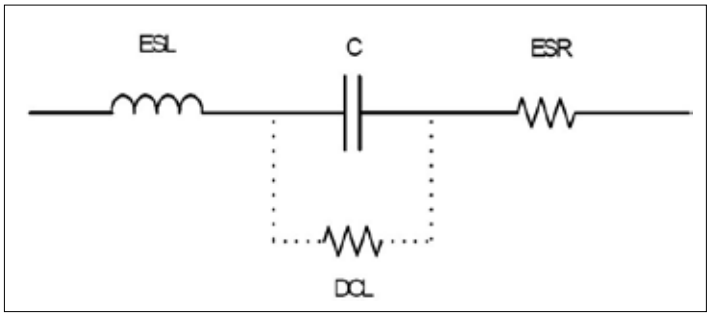

Figure 7: Capacitor electrical model.

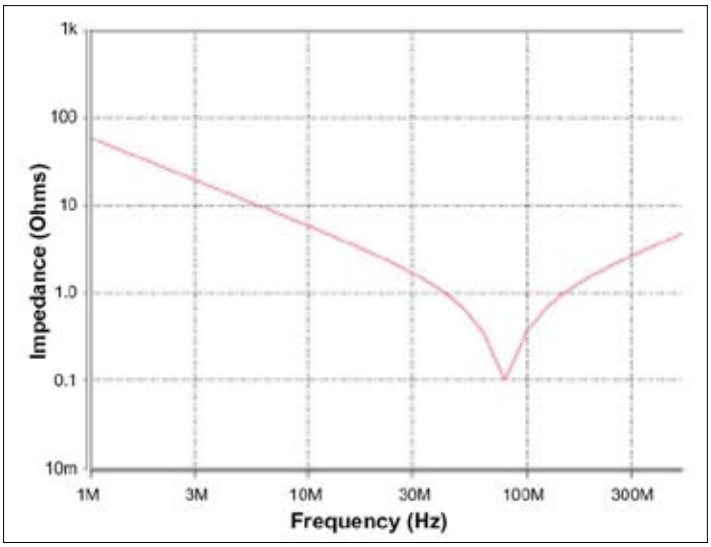

Figure 8. Impedance vs. frequency plot.

resonant frequency of the capacitor and inductor. Beyond this frequency, the circuit behaves like an inductor and not a capacitor. It is imperative that the capacitor selected for CL have a self-resonant frequency much higher than the sampling frequency to perform the required function.

Capacitance versus voltage is another important capacitor attribute that must be considered to minimize distortion. Several common capacitor types have a nonlinear characteristic where the capacitance varies as a function of the applied voltage. This typically results from the type of dielectric used in the manufacture of the capacitor.

Capacitors designed for power supply decoupling, such as X7R and Z5U, are generally inexpensive but exhibit this type of behavior. Capacitor characteristics are generally dictated by the dielectric employed and the mechanical or physical attributes of the device. These details are beyond the scope of this paper but suffice it to say, not all capacitors are created equal. As a recommendation, COG capacitors are generally preferred due to low inductance and a very linear capacitance versus voltage characteristic.

Physically positioning CL near the A/D input pins on the printed circuit board is critical to performance for a couple of reasons. First, refer to figure 7 and the equivalent series inductance in the electrical model of the capacitor.

It is important to realize that when CL is placed on the circuit board, the equivalent series inductance of the capacitor is in series with the inductance of the internal bonding wire which connects the IC pin to the integrated circuit, typically 1 nH, and the inductance of the printed circuit board (PCB) trace from the capacitor to the IC pin, which is 10 nH per inch. The inductance of the PCB trace can easily become the dominant inductance of the circuit, which will effectively lower the self-resonant frequency of the circuit, and the effectiveness of CL, if improperly placed.